Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 80019

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2025
Third Semester
Electrical and Electronics Engineering
U23EE305 – DIGITAL LOGIC CIRCUITS
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

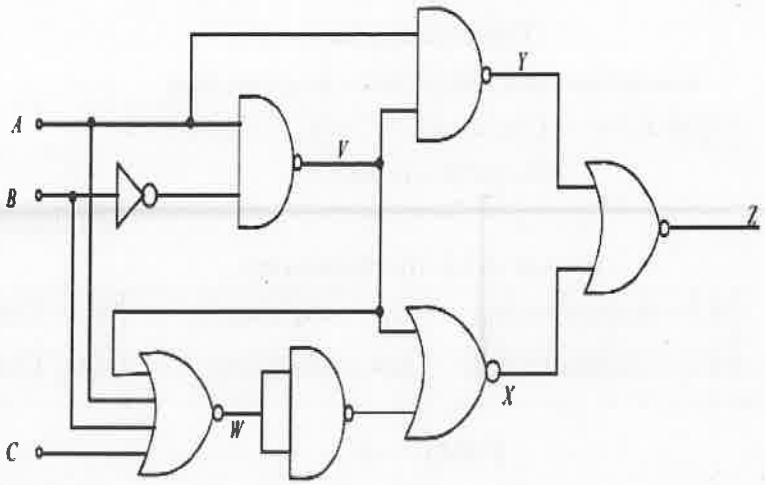
(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Consider two 8-bit binary numbers, P = 11101101 and Q = 11100110, perform the subtraction P − Q using signed 2's complement representation.	2	K2	CO1
2.	Compare the CMOS and TTL logic families with respect to the following parameters i) Propagation delay ii) Power dissipation iii) Fan-out	2	K2	CO1
3.	Write the Boolean expressions for the sum and carry outputs of a full adder circuit.	2	K1	CO2
4.	Justify why NAND and NOR gates are referred to as universal gates.	2	K2	CO2
5.	Identify the selection lines and inputs required to implement the Boolean function F(A, B, C, D) = Σm(0, 3, 4, 7, 9, 13, 15) using a 4×1 multiplexer.	2	K2	CO3
6.	List any four applications of decoder in digital systems.	2	K1	CO3
7.	How does the master-slave JK flip-flop eliminate the race around condition?	2	K2	CO4
8.	Give the logic diagram and characteristic table of the flip-flop commonly used in counter design.	2	K2	CO4
9.	Classify Asynchronous sequential circuits.	2	K2	CO5
10.	Compare and contrast static hazards and dynamic hazards in asynchronous circuits.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	A combinational logic circuit is shown in Fig. 1. Obtain a simplified Boolean expression for this circuit at V, W, X, Y and Z in terms of input variables A, B and C.	13	K2	CO1



(OR)

	b)	The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word. (Assume even-parity) Message: 1001001, 1001110, 0110111, 1101100	13	K2	CO1
12.	a)	Given the Boolean function F = A + B'C, i. Express the function in SOP form ii. List the truth table for the function iii. Identify the minterms and iv. Implement the SOP logic using NAND gates	13	K3	CO2

(OR)

	b)	Using the Quine-McCluskey method, simplify the Boolean function F(A, B, C, D) = Σm(0, 1, 2, 5, 7, 8, 9, 10, 13, 15). Also, realize the minimized expression using appropriate logic gates.	13	K3	CO2
13.	a)	Construct a 3 x 8 decoder using basic logic gates. Explain how the full adder can be implemented using a decoder?	13	K2	CO3

(OR)

	b)	Realize the following Boolean function using an 8×1 multiplexer. F(w, x, y, z) = Σ(1, 4, 6, 7, 8, 9, 10, 11, 15)	13	K3	CO3

14.	a)	Explain the step-by-step procedure used to implement the Mod-10 synchronous counter using D flip-flops.	13	K2	CO4
		(OR)			
	b)	Build a 3-bit synchronous up/down counter. Provide the truth table, control logic, and logic diagram.	13	K2	CO4
15.	a)	Consider a sequential circuit consists of two D flip-flops A and B with two inputs X and Y, and output Z is specified by the following equations: DA = X'A + XY DB = X'A + XB Z = XB i. Draw the logic diagram of the circuit. ii. Construct the state table and derive the corresponding state diagram.	13	K4	CO5
		(OR)			
	b)	Analyze the impact of race conditions in asynchronous sequential circuits. How does the races affect circuit behavior and reliability illustrate with an example?	13	K4	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Design a combinational circuit to compare two 4-bit binary numbers A and B. The circuit should produce three output binary signals indicating whether A > B, A = B, or A < B.	15	K3	CO3
		(OR)			
	b)	Assume that there is parking area in a shop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car, which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip-flops to monitor the number of cars entering the parking area. Also, determine the minimum number of flip-flops are required if the parking capacity is increased to 50 cars. Justify your answer.	15	K2	CO4